PI3WVR12612
PI3WVR12612 DP/HDMI Application Information

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1 Introduction

PI3WVR12612 is a 4-lane DP and HDMI video switch, which can support 5.4Gbps data rate. On top of video signals, HPD and DP AUX/DDC can be switched through PI3WVR12612. PI3WVR12612 is used to connect one or two DP/HDMI source device(s) to two or one DP/HDMI sink device(s). PI3WVR12612 for 1:2 dual-mode DP source and 2:1 HDMI sink application circuits are described in this document.

2 Typical Application Circuit

PI3WVR12612 is designed to transmit DP main link signals, which are delivered from a source with up to 2.0V Vbias_TX in source application per DP Standard Version 1.2. It is also capable to transmit HDMI TMDS signals which are terminated at 3.3V AVcc per HDMI Specification Version 1.4.

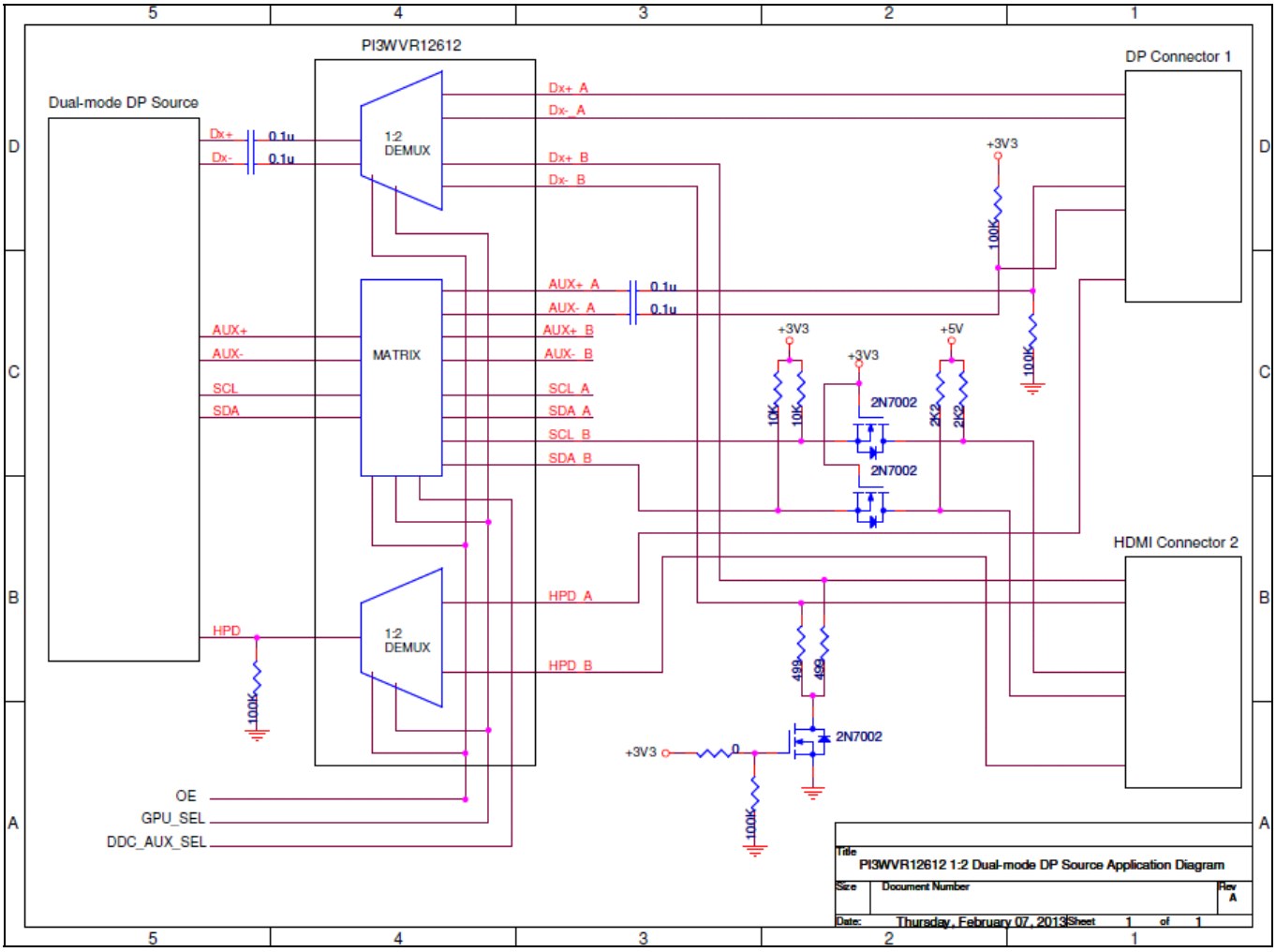

Figure 1: PI3WVR12612 1:2 Dual-Mode DP Source Application Diagram

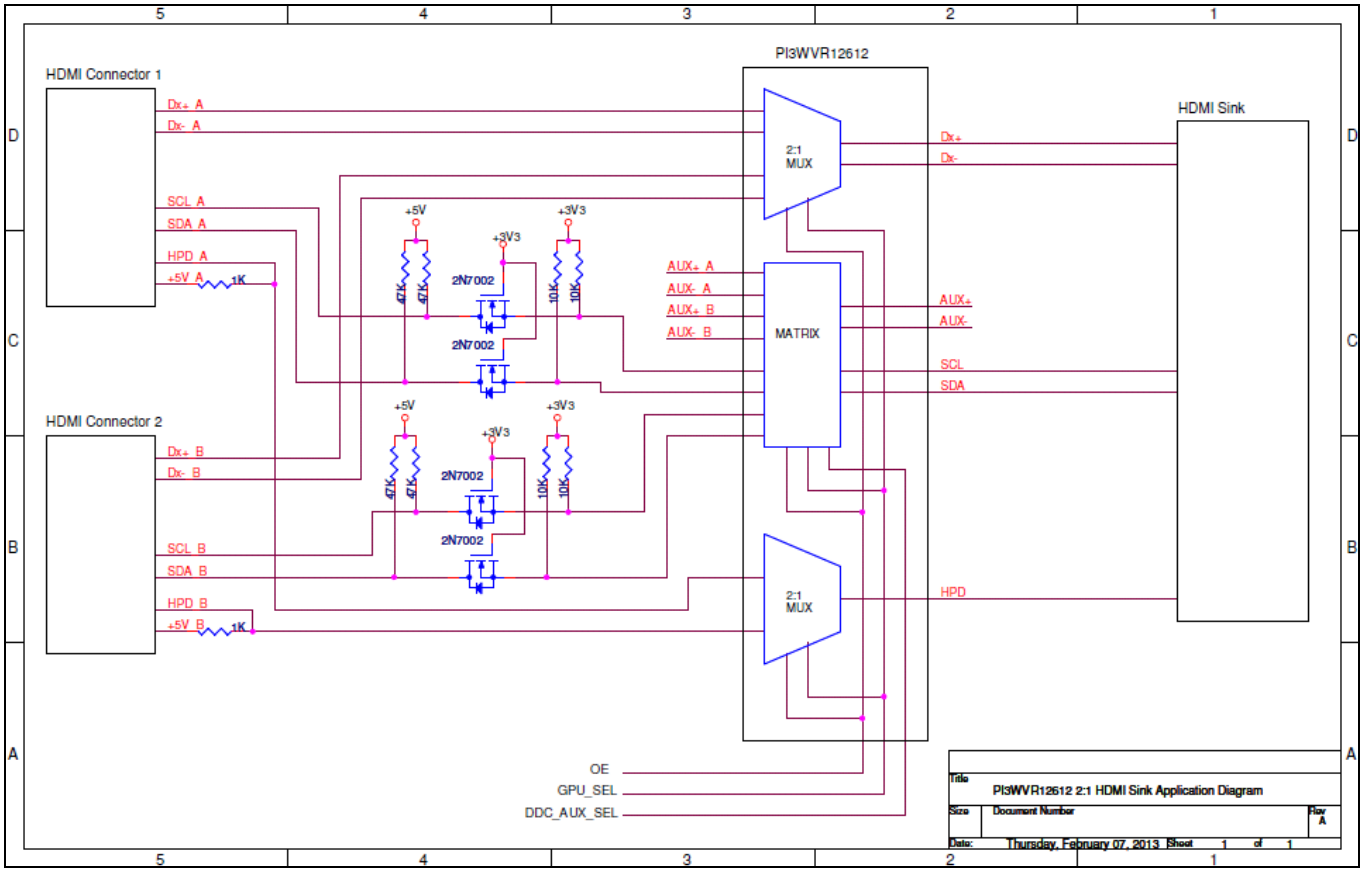

Figure 2: PI3WVR12612 2:1 HDMI Sink Application Diagram

2.1 Main Link Channels

In source application, AC coupling capacitors at all main link signals are inserted per DP Standard Version 1.2. AC coupling capacitor value in the range of 75 – 200nF is required. Per HDMI architecture, a 499Ω pull-down resistor should be implemented at each TMDS trace so as to create a proper DC offset in a dual-mode DP source circuit. A FET can be used to enable all 499Ω pull-down resistors.

2.2 AUX Channels

Per DP Standard Version 1.2, AC coupling capacitor value in the range of 75 – 200nF is also required for each AUX signal. After the AC coupling capacitor, source is required to pull AUX+ to GND and AUX- to DP_PWR via resistors in the range of 10kΩ to 105kΩ in source application. 100kΩ resistor value is recommended per DP Standard Version 1.2. When a DP sink device determines AUX+ and AUX- being pulled to low and high, respectively, a DP source device is connected.

2.3 DDC Channels

Per HDMI Specification Version 1.4, each of SCL and SDA is pulled up to 5V via a resistor in the range of 1.5kΩ to 2kΩ in source application or via a resistor of 47kΩ in sink application. As DDC design of PI3WVR12612 is for 3.3V transmission, FET is implemented to isolate 3.3V at PI3WVR12612 device side from 5V at HDMI connector side.

2.4 HPD Signal

A weak, pull-down resistor, 100kΩ for instance, is normally implemented at HPD in order to have a known state for dual-mode DP source device when no sink device is attached to it.

Per HDMI Specification Version 1.4, HPD should be pulled to 5V via a 1kΩ resistor for sink application. This is to signal an HDMI source device a sink device is attached.

2.5 Control Pins

GPU_SEL pin of PI3WVR12612 is used to select high-speed signal port. DDC_AUX_SEL pin is to define to which paths AUX and DDC should be switched. GPU_SEL and DDC_AUX_SEL can be connected to GPIOs to do the selections.

OE pin of PI3WVR12612 is active high. For normal operation, it can be connected to VDD via a weak pull-up resistor. Alternatively, it can be controlled by a GPIO.

3 Layout Design Guideline

Layout guideline especially for high-speed transmission is critical. Please refer to PIxxxx High Speed Layout Guideline for detailed recommendations.

4 References

(1) VESA DisplayPort Standard Version 1 Revision 2, Video Electronics Standards Association, January 5, 2010
(2) VESA DisplayPort Dual-Mode Standard Version 1, Video Electronics Standards Association, February 10, 2012
(3) VESA DisplayPort Interoperability Guideline Version 1.1a, Video Electronics Standards Association, February 5, 2009
(4) High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC, June 5, 2009
(5) PCI Express Board Design Guidelines Draft, Intel Corporation, June 2003